Amendments to the Specification

Please replace paragraph **[0087]** with the following rewritten paragraph:

[0087] FIG. 11 is an explanatory diagram showing the pixel structure of the first example and corresponds to FIG. 4. FIG. 11 is almost same as FIG. 4. In pixels 112A, however, an n-region 210A that functions as the substrate region of the clear transistor CTr is different from the n-region 210 of the pixels 112. Specifically, the n-region 210A formed below the clear gate 270C includes an interface region 210b having a relatively low impurity concentration in the vicinity of the interface between the gate insulating film 260C and the n-region 210A. In other words, the substrate region 210A of the clear transistor CTr includes an upper region (interface region 210b) formed in the vicinity of the clear gate 270C and having a relatively low impurity concentration, and a lower region 210b[1] formed below the upper region and having a relatively high impurity concentration. In this structure, the clear transistor CTr is set to be in an "on" state with the source voltage CVs at the time when generated holes spill from the first p-region 220, since the threshold voltage CVth of the clear transistor is set to be relatively low.